

ABSTRACT OF THE DISCLOSURE

A teacher-pupil flip-flop with reduced register delay including a gate circuit, a stack circuit, a keeper circuit, a teacher output circuit, a latch circuit and a pupil output circuit. The gate circuit switches after a setup delay in response to transitions of a clock signal. The stack circuit, coupled to the gate circuit output and to an input, switches an intermediate node pair to a preliminary state when the clock signal is low, and to a data state indicative of the input after the setup delay when the clock signal goes high. The keeper circuit maintains the data state and the teacher output circuit drives the output based on the data state while the clock is high. The latch circuit stores the data state and the pupil output circuit drives the output with valid data from the latch circuit after the clock signal goes low.